REMARKS/ARGUMENTS

Claims 1-15 and 17-61 are pending in the application, claims 25-36 and 55-61 are withdrawn, and claims 1, 3, 10, 37, 45, 46, 51, and 53 are amended. As discussed below, all of the claims are in condition for allowance. **But if after considering this response the Examiner does not allow all of the claims, then the Applicants' attorney requests that the Examiner contact him to schedule and conduct a telephone interview before issuing a subsequent Office Action.**

The Phone Interview With The Examiner On January 21, 2010

The Applicants' attorney thanks the Examiner for participating in a telephone interview on January 21, 2010.

During the interview, the Applicants' attorney and the Examiner discussed claims 1, 10, and 37, specifically the Examiner's interpretation of some of the limitations of these claims and potential ways to amend these limitations to define over the art in the Examiner's opinion. But no agreement was reached.

Information Disclosure Statement

The Applicant's attorney encloses a corrected Information Disclosure Statement form for the reference "Matlab to RTL Synthesis", and, therefore, requests that the Examiner consider this reference, and indicate his consideration of this reference by returning a signed or initialed copy of the corrected IDS form.

Objections To The Specification

The Applicants' attorney continues to believe that the amended title of the application submitted in a response filed 19 December 2007 is descriptive of the claimed invention. But the Applicants' attorney will contemplate an amended title, and requests the Examiner's patience while he does so.

Rejection Of Claims 10-12, 14-15, 17-18, 37, 39-43, 45, and 47-49 Under 35 U.S.C. § 102(b) As Being Anticipated By U.S. Patent 4,703,475 To Dretzka

Claim 10

Claim 10 as amended recites a processor operable to generate data that includes only non-data-destination information, retrieve the generated data, load the retrieved data into a buffer, unload the data from the buffer, and process the unloaded data such that the processed data includes only non-data-destination information.

For example, referring, *e.g.*, to FIGS. 3-5 and paragraph [82] of the patent application, in an embodiment, a processor 42 is operable to generate data under the control of a first thread 100_3 of an application 80, the generated data including only non-data-destination information. The processor 42 is further operable to load the data into a buffer 106_5 under the control of a data-transfer object 86_{5a}, unload the data from the buffer 106_5 under the control of a second data-transfer object 86_{5b}, and process the unloaded data under the control of a second thread 100_4 of the same application 80 such that the processed data includes only non-data-destination information.

In contrast, Dretzka does not disclose a processor operable to generate data that includes only non-data-destination information, retrieve the generated data and load the retrieved data into a buffer, unload the data from the buffer, and process the unloaded data such that the processed data includes only non-data-destination information. In response to the Examiner's first interpretation of Dreztka on p. 6 of the office action, even if Dreztka's processor 21 (FIG. 2) can be considered to "generate" a data packet in the input list 230-4, this "generated" data packet includes a 3-byte packet header (FIG. 17) having information regarding a destination (*e.g.*, the logical channel LCN) of the data packet (*e.g.*, col. 7, lines 35-38 and lines 45-53, and col. 9, line 60 – col. 10, line 11). And in response to the Examiner's second interpretation of Dreztka on pp. 9-10 of the office action, even if Dreztka's processor 11 (FIG. 2) can be considered to "process" a data packet unloaded from the buffer 120-4 (FIG. 5), the resulting unloaded and

processed data packet includes a 3-byte packet header (FIG. 17) having information regarding a destination (*e.g.*, the logical channel LCN) of the data packet (*e.g.*, col. 7, lines 35-38, and col. 8, line 55 – col. 9, line 12).

In the office action, the Examiner focuses on only the 1-byte multilink header, and ignores the 3-byte packet header. But because the 3-byte packet header includes information regarding a destination (the LCN) of the data packet, the Examiner's rejection is improper.

During the above-mentioned telephone interview, the Examiner said he would not allow claim 10 with a negative claim limitation. So the Applicants' attorney has amended claim 10 to remove the negative claim limitation.

Furthermore, during the telephone interview the Examiner admitted he had not considered Dretzka's 3-byte packet header, and, therefore, would reconsider claim 10 in view of the above argument that the 3-byte packet header includes data-destination information.

Claims 11-12, 14-15, and 17-18

These claims are patentable by virtue of their respective dependencies from claim 10.

Claim 37

Claim 37 recites loading data published with an application into a first buffer, the loaded data consisting only of non-data-destination information, each location within the buffer corresponding to a same data destination, and retrieving the published data from the buffer, the retrieved data consisting only of non-data-destination information.

For example, referring, *e.g.*, to FIGS 3-5 and paragraphs [66] – [70] of the patent application, in an embodiment a thread 100_1 of an application 80 publishes data that consists only of non-data-destination information, and a data-transfer object 86_{1a} loads the published data into a buffer 106_1, the loaded data consisting only of

non-data-destination information. Each location within the buffer corresponds to a same data destination or to same data destinations. Then another data-transfer object 86_{1b} retrieves the published data from the buffer, the retrieved data consisting only of non-data-destination information. Next, because the channel 104_1 corresponds to one or more specified destinations, the data-transfer object 86_{1b} adds to the published data information (*e.g.*, a header) indicating the destination(s) of the published data. This relieves the application 80 and the thread 100_1 of the burden of adding destination information to the published data.

In contrast, Dretzka does not disclose loading data published with an application into a first buffer, each location within the buffer corresponding to a same data destination, the loaded data consisting only of non-data-destination information, and retrieving the published data from the buffer, the retrieved data consisting only of non-data-destination information. In response to the Examiner's interpretation on p. 14 of the office action, data loaded into a buffer 120-4 (FIG. 5) includes a 3-byte packet header (*e.g.*, col. 8, lines 55-65, and FIG. 17), which identifies a logic channel LCN (destination) to which the data is assigned. Furthermore, data retrieved from the buffer 120-4 includes the same 3-byte packet header (e.g., col. 8, line 65 – col. 9, line 4). Analogous arguments apply to the buffers 130. And the message queue 110 cannot be the "first buffer" because not all of the locations within the message queue correspond to a same LCN (*e.g.*, col. 7, lines 25-30).

In the office action, the Examiner focuses on only the 1-byte multilink header, and ignores the 3-byte packet header. But because the 3-byte packet header includes information regarding a destination (the LCN) of the data packet, the Examiner's rejection is improper.

During the above-mentioned telephone interview, the Examiner said he would not allow claim 37 with a negative claim limitation. So the Applicants' attorney has amended claim 37 to remove the negative claim limitation.

Furthermore, during the telephone interview the Examiner admitted he had not considered Dretzka's 3-byte packet header, and, therefore, would reconsider claim 37 in

view of the above argument that the 3-byte packet header includes data-destination information.

Claims 39-43

These claims are patentable by virtue of their respective dependencies from claim 37.

Claim 45

Claim 45 recites receiving a message that includes data and that includes a message header that indicates a destination of the data, the destination corresponding to a software application, and loading into a first buffer the received data with no message header, the first buffer corresponding to the destination

For example, referring, *e.g.*, to FIGS. 3-5 and paragraphs [76] – [77], in an embodiment a communication object 88 receives from a pipeline bus 50 a message that includes data and that includes a message header that indicates a destination of the data, the destinations being the software-application threads 100_1 and 100_2 (corresponding to a software application). A data-transfer object 86_{2b} strips the message header from the message and loads the data (without the stripped message header) into a buffer 106_2 that corresponds to the application threads 100_1 and 100_2, which are the destinations of the data.

In contrast, Dretzka does not disclose loading into a buffer received data with no message header, the buffer corresponding to a destination of the data, the destination corresponding to a software application. In response to the Examiner's interpretation on p. 16 of the office action, received data loaded into the buffer 220-4 (FIG. 6) includes a 3-byte header (*e.g.*, FIG. 4, col. 10, lines 1-11), which identifies a logic channel LCN (destination) to which the data is assigned.

In the office action, the Examiner focuses on only the 1-byte multilink header, and ignores the 3-byte packet header. But because the 3-byte packet header includes

information indicating a destination (the LCN) of the data packet, the Examiner's rejection is improper.

Claims 47-49

These claims are patentable by virtue of their respective dependencies from claim 45.

Rejection Of Claims 1-3 And 5-9 Under 35 U.S.C. § 103(a) As Being Obvious Over Dretzka In View Of U.S. 6,985,975 To Chamdani

Claim 1

Claim 1 as amended recites first and second parallel buffers respectively associated with first and second data-processing units, and a processor operable to load at least a portion of published data into the first buffer and to load at least the same portion of the published data into the second buffer.

For example, referring, *e.g.*, to FIGS. 3-5 and paragraphs [67] – [72] and [83] of the patent application, in an embodiment, a processor 42 is operable, under the control of an application thread 100_3, to publish data, and is operable, under the control of data-transfer object 86_{3a}, to load at least a portion of the published data into a first buffer 106_3, which is associated with a first data-processing unit (*e.g.*, a first hardwired pipeline 74) within the pipeline accelerator 44, and is operable, under the control of data-transfer object 86_{5a}, to load at least the same portion of the published data into a second buffer 106_5, which is associated with a second data-processing unit (*e.g.*, a second hardwired pipeline 74) within the pipeline accelerator and which is parallel to the first buffer 106_3.

In contrast, Dretzka does not include first and second parallel buffers respectively associated with first and second data-processing units, and a processor operable to load at least a portion of published data into the first buffer and to load at least the same

portion of the published data into the second buffer as recited in claim 1. Referring to FIG. 5, even if the buffers, *e.g.*, 120-0 and 120-4, can be considered parallel and to be associated with different data-processing units, the processor 11 does not load the same data into these buffers.

And neither does Chamdani disclose first and second parallel buffers respectively associated with first and second data-processing units. In contrast, Chamdani's buffers (*e.g.*, FIFOs 102 and 103) are associated with a same data-processing unit (*e.g.*, whatever data-processing unit is connected to the single output of the coupler 110, and FIG. 5, step 408).

Consequently, the combination of Dretzka and Chamdani would at most suggest duplicating, for example, Dretzka's buffer 120-0, for redundancy, and loading these two buffers with the same data. But, unlike the first and second buffers recited in claim 1, the two buffers 120-0 would still be associated with only a single data-processing unit.

During the telephone interview, the Examiner stated that he interpreted "data-processing destination" to include the first and second buffers, but that amending "data-processing destination" to "data-processing unit" may overcome this rejection.

Claims 2-3 and 5-9

These claims are patentable by virtue of their dependencies from claim 1.

Rejection Of Claim 4 Under 35 U.S.C. § 103(a) As Being Obvious Over Dretzka In View Of Chamdani And Further In View Of The Examiner's Taking Of Official Notice

Claim 4

Claim 4 is patentable by virtue of its dependency from claim 1.

Furthermore, the Applicants' attorney objects to the Examiner's taking of official notice.

Even though threaded processing may be known, it generally requires a processor with certain attributes, such as parallel execution paths and/or time sharing of a single execution path.

Because both Dretzka and Chamdani are silent as to threaded processing, there is no teaching in any of the cited references as to how one would modify Dretzka and Chamdani to include threaded processing, if the processors of Dretzka and Chamdani are capable of threaded processing, or if the architectures of Dretzka and Chamdani are even compatible with threaded processing.

Consequently, the Examiner must cite another reference that teaches if and how one can modify the circuitry of Dretzka and Chamdani to implement threaded processing; merely taking official notice is insufficient to provide this teaching.

Rejection Of Claims 13-14, 38, 44, 46, And 50 Under 35 U.S.C. § 103(a) As Being Obvious Over Dretzka In View Of The Examiner's Taking Of Official Notice

Claim 13

Claim 13 is patentable by virtue of its dependency from claim 10.

Furthermore, the Applicants' attorney objects to the Examiner's taking of official notice.

Even though threaded processing may be known, it generally requires a processor with certain attributes, such as parallel execution paths and/or time sharing of a single execution path.

Because Dretzka is silent as to threaded processing, there is no teaching in any of the cited references as to how one would modify Dretzka to include threaded processing, if the processors of Dretzka are capable of threaded processing, or if the architecture of Dretzka is even compatible with threaded processing.

Consequently, the Examiner must cite another reference that teaches if and how one can modify the circuitry of Dretzka to implement threaded processing; merely taking

official notice is insufficient to provide this teaching.

Claim 14

Claim 14 is patentable by virtue of its dependency from claim 10.

Claim 38

Claim 38 is patentable by virtue of its dependency from claim 37.

Furthermore, the Applicants' attorney objects to the Examiner's taking of official notice for the reasons discussed above in conjunction with claim 13.

Claim 44

Claim 44 as amended is patentable by virtue of its dependency from claim 37.

Furthermore, the amendment to claim 44 renders the Examiner's taking of official notice moot.

Claim 46

Claim 46 is patentable by virtue of its dependency from claim 45.

Furthermore, the Applicants' attorney objects to the Examiner's taking of official notice for the reasons discussed above in conjunction with claim 13.

Claim 50

Claim 50 is patentable by virtue of its dependency from claim 45.

Furthermore, the amendment to claim 50 renders the Examiner's taking of official notice moot.

Rejection Of Claims 19-24 and 51-54 Under 35 U.S.C. § 103(a) As Being Obvious Over Dretzka In View Of U.S. Patent 6,216,191 to Britton

Claim 19

Claim 19 recites a pipeline accelerator that includes a destination of data and that is operable to receive a message that includes information indicating the destination, to recover the data from the message, and to process the recovered data at the destination without executing a program instruction.

For example, referring, *e.g.,* to FIGS. 3-5 and paragraphs [67] – [72] of the patent application, in an embodiment, a processor 42 constructs a message that includes data and information indicating a destination of the data within a pipeline accelerator 44, and drives the message onto a bus 50. The accelerator 44 is operable to receive the message from the bus 50, to recover the data from the message, and to process the recovered data at the destination without executing a program instruction.

In contrast, neither Dreztka nor Britton, viewed alone or in combination, discloses a pipeline accelerator that includes a destination of data and that is operable to receive a message that includes information indicating the destination, to recover the data from the message, and to process the recovered data at the destination without executing a program instruction.

The Examiner admits on p. 26 of the Office Action that Dretzka lacks this limitation.

Furthermore, referring, *e.g.,* to FIGS. 1-3, Britton does not disclose or suggest a pipeline accelerator that is operable to receive a message that includes information indicating a destination of data and to recover data from the message. Britton merely discloses an FPGA that communicates with a processor 102 via a combined address and data bus AD or separate address and data busses A and D.

Therefore, because Britton discloses an FPGA having an address-bus/data-bus interface and lacking a message-based interface as recited in claim 19, the Examiner

has failed to make a prima facie showing of obviousness. That is, there is no teaching or suggestion in Britton as to how one would modify his FPGA to receive messages.

Furthermore, because Dretzka discloses a message-based interface and Britton discloses an address-bus/data-bus interface, one of ordinary skill would not have been motivated to combine Dretzka and Britton to arrive at the subject matter recited in claim 19.

And even if one were motivated to combine Dretzka and Britton, neither Dretzka nor Britton discloses or suggests how one would modify Britton's address-bus/data-bus interface to communicate with Dretzka's message-based interface. And such modification was likely impossible because at the time Britton was filed, it is unlikely that available FPGAs included a sufficient number of gates to instantiate a message-based interface that would be compatible with Dretzka's message-based interface.

Consequently, the combination of Dretzka and Britton does not render claim 19 obvious.

Claims 20-21

These claims are patentable by virtue of their dependencies from claim 19.

Claim 22

Claim 22 recites a pipeline accelerator operable to generate data without executing a program instruction, to generate a header including information indicating a destination of the data, and to package the data and header into a message.

Referring, e.g., to FIG. 3, paragraph [49], and paragraph [74] of the patent application, a pipeline accelerator 44 is operable to generate data without executing a program instruction, to generate a header including information indicating a destination of the data (e.g., a thread 100 of an application program 80 of FIG. 5), to package the data and header into a message, and to drive the message onto a bus 50.

In contrast, neither Dretzka nor Britton, viewed alone or in combination, discloses

or suggests a pipeline accelerator operable to generate data without executing a program instruction, to generate a header including information indicating a destination of the data, and to package the data and header into a message.

The Examiner admits on p. 29 of the Office Action that Dretzka lacks this limitation.

Furthermore, referring, e.g., to FIGS. 1-3, Britton does not disclose or suggest a pipeline accelerator that is operable to generate a header including information indicating a destination of data and to package the data and header into a message. Britton merely discloses an FPGA that communicates with a processor 102 via a combined address and data bus AD or separate address and data busses A and D.

Therefore, because Britton discloses an FPGA having an address-bus/data-bus interface and lacking a message-based interface as recited in claim 22, the Examiner has failed to make a prima facie showing of obviousness. That is, there is no teaching or suggestion in Britton as to how one would modify his FPGA to receive messages.

Furthermore, because Dretzka discloses a message-based interface and Britton discloses an address-bus/data-bus interface, one of ordinary skill would not have been motivated to combine Dretzka and Britton to arrive at the subject matter recited in claim 22.

And even if one were motivated to combine Dretzka and Britton, neither Dretzka nor Britton discloses or suggests how one would modify Britton's address-bus/data-bus interface to communicate with Dretzka's message-based interface. And such modification was likely impossible because at the time Britton was filed, it is unlikely that available FPGAs included a sufficient number of gates to instantiate a message-based interface that would be compatible with Dretzka's message-based interface.

Consequently, the combination of Dretzka and Britton does not render claim 22 obvious.

Claims 23-24

These claims are patentable by virtue of their dependencies from claim 22.

Claim 51

Claim 51 recites receiving a message including data and information that indicates a destination of the data and processing the data with a pipeline accelerator that includes a field-programmable gate array.

In contrast, neither Dreztka nor Britton, viewed alone or in combination, discloses receiving a message including data and information that indicates a destination of data and processing the data with a pipeline accelerator that includes a field-programmable gate array.

The Examiner admits on p. 31 of the Office Action that Dretzka lacks this limitation.

Furthermore, referring, *e.g.*, to FIGS. 1-3, Britton does not disclose or suggest a pipeline accelerator that is operable to receive a message that includes data and information indicating a destination of that data. Britton merely discloses an FPGA that communicates with a processor 102 via a combined address and data bus AD or separate address and data busses A and D.

Therefore, because Britton discloses an FPGA that has an address-bus/data-bus interface that lacks the ability to receive a message as recited in claim 51, the Examiner has failed to make a prima facie showing of obviousness. That is, there is no teaching or suggestion in Britton as to how one would modify his FPGA to receive messages.

Furthermore, because Dretzka discloses a message-based interface and Britton discloses an address-bus/data-bus interface, one of ordinary skill would not have been motivated to combine Dretzka and Britton to arrive at the subject matter recited in claim 51.

And even if one were motivated to combine Dretzka and Britton, neither Dretzka nor Britton discloses or suggests how one would modify Britton's address-bus/data-bus

interface to receive messages from Dretzka's message-based interface. And such modification was likely impossible because at the time Britton was filed, it is unlikely that available FPGAs included a sufficient number of gates to instantiate a message-based interface that would be compatible with Dretzka's message-based interface.

Consequently, the combination of Dretzka and Britton does not render claim 51 obvious.

Claim 52

Claim 52 is patentable by virtue of its dependency from claim 51.

Claim 53

Claim 53 as amended recites generating with a pipeline accelerator and without executing a program instruction a message header that includes a destination of data and a message that includes the header and the data.

Dretzka does not disclose performing any function without executing a program instruction.

Furthermore, referring, *e.g.*, to FIGS. 1-3, Britton does not disclose or suggest a pipeline accelerator that is operable to generate a message header that includes a destination of data and a message that includes the header and the data. Britton merely discloses an FPGA that communicates with a processor 102 via a combined address and data bus AD or separate address and data busses A and D.

Therefore, because Britton discloses an FPGA that has an address-bus/data-bus interface and that lacks the ability to generate a message header that includes a destination of data and a message that includes the header and the data as recited in claim 53, the Examiner has failed to make a prima facie showing of obviousness. That is, there is no teaching or suggestion in Britton as to how one would modify his FPGA to generate messages.

Furthermore, because Dretzka discloses a message-based interface and Britton

discloses an address-bus/data-bus interface, one of ordinary skill would not have been motivated to combine Dretzka and Britton to arrive at the subject matter recited in claim 53.

And even if one were motivated to combine Dretzka and Britton, neither Dretzka nor Britton discloses or suggests how one would modify Britton's address-bus/data-bus interface to communicate with Dretzka's message-based interface. And such modification was likely impossible because at the time Britton was filed, it is unlikely that available FPGAs included a sufficient number of gates to instantiate a message-based interface that would be compatible with Dretzka's message-based interface.

Consequently, the combination of Dretzka and Britton does not render claim 53 obvious.

Claim 54

Claim 54 is patentable by virtue of its dependency from claim 53.

CONCLUSION

In view of the foregoing, claims 2, 4-9, 11-15, 17-24, 38-43, 47-49, 52, and 54 as previously pending, and claims 1,3, 10, 37, 45, 46, 51, and 53 as amended are in condition for allowance. Therefore, the issuance of a formal Notice of Allowance at an early date is respectfully requested. **If the Examiner does not agree that all claims are in condition for allowance, the Examiner is respectfully requested to telephone the undersigned prior to issuing an action rejecting the claims to schedule a telephone interview.**

In the event additional fees are due as a result of this amendment, you are hereby authorized to charge such payment to Deposit Account No. 07-1897.

DATED this 17th day of February 2010.

Respectfully submitted,

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